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EXAMINER

E1M1/0929

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ART UNIT	PAPER NUMBER
2104	8

DATE MAILED: 09/29/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 6-23-97 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-13, 15, 17-23 and 25-26 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☒ Claims 14, 16 and 24 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-13, 15, 17-23, 25 and 26 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☒ The proposed drawing correction, filed 6-23-97, has been ☒ approved; ☐ disapproved (see explanation).
12. ☒ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☒ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the specific diode connections of Claim 11 must be shown or the feature(s) cancelled from the claim. No new matter should be entered.

*** The following rejection has been maintained from the Office Action of 2-20-97.

2. Claims 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Pianka (5,345,357).

Pianka discloses (Fig. 2) a circuit comprising a first transistor (201) having a first terminal coupled to a first supply voltage (VDD) and a second terminal connected to a supply voltage (VSS) through (202), a second transistor (204) having a first terminal connected to a third terminal of the first transistor through (203) and a second terminal connected to said second supply voltage through (202) and a capacitor (205) connected between a third terminal of said second transistor and said first supply voltage through (208, 209).

*** The following rejection includes the new rejection of Claim 26.

3. Claims 9, 10, 18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pianka.

Pianka discloses the use of a second resistor (206), but does not disclose the use of a first resistor being coupled between the third terminal of the first transistor and the first voltage supply. However, the use of the second resistor would have been obvious as a mere matter of engineering design choice. The second resistor, its connection between the gate and the first voltage supply and its value merely alter

the biasing of the transistor and dismissing added space and cost requirements, would have been obvious to use so as to obtain the desired operating parameters of the circuit. As far as the limitations found in Claim 26, bond pad (200) could reasonably be interpreted as a supply of power since protection is offered to this terminal against voltage surges "exceeding a desired limit"; "desired limit" alludes to there being some accepted supply of power at the terminal. See col. 4, lines 55-61, wherein there is suggestion for application to offering protection against surges occurring upon a power supply terminal. Therefore, it is the position of the Examiner that it would have been obvious to one having ordinary skill in the art at the time of the invention to apply the teachings of Pianka to any terminal, such as, a terminal of a power supply so as to protect components and circuitry from overage conditions thereby increasing the overall circuit reliability.

4. Claims 1-6, 8, 11, 13 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pianka in view of Koepp (3,636,385).

These claims essentially add the limitations that the first transistor be of one type and the second transistor be of the second type, the use of a diode and specific connections with respect to the sources and the drains of the transistors. Pianka discloses that the first (201) and second (204) transistors are of the same type (n-channel), but that the protection circuit may be implemented utilizing (p-channel) MOSFETs and/or CMOS output buffers (i.e. 201-p, 202-n). Such changes would merely require such changes as reverse supply

connections and etc...; the changes would be well within the abilities of one having ordinary skill in the art (col. 2, lines 29-68 and col. 5, lines 12-36). Koepp teaches (Fig. 1) a device for protecting a circuit wherein it is known to use a first transistor of a first type (16 p-channel), a second transistor of a second type (36 n-channel) coupled between the third terminal of the first transistor and a second supply (28) and the use of a diode (56). It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teachings Koepp and the disclosure of Pianka, as a matter of engineering design choice, in order to offer protection from any number of transient conditions, positive and negative, occurring at any supply terminal, while meeting the biasing and operating parameters of the circuit application, such as the voltage levels for transistor conduction and non-conduction thereby resulting in a highly reliable end-product.

5. Claims 15, 17, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banura in view of Merrill (5,239,440).

Banura discloses (Fig. 4) a device from protecting a circuit against surges wherein there is a first transistor (T3), a second transistor (T2), a third transistor (T1), a first power supply (+27v) and a second power supply (GND). These claims essentially require that the third terminal of the third transistor be connected to the first power supply through a capacitor and that the transistors are NPN bipolar transistors. Banura further discloses the use of both NPN and PNP type bipolar transistors and the use of one type over the other would have been obvious as a mere matter of engineering design choice

and well within the abilities of one having ordinary skill. These choices depend merely upon such considerations as whether one uses a negative or positive power supply for operation of the remaining circuitry. As to the use of a capacitor, Banura discloses the use of a sensing resistor for triggering, but Merrill teaches in Figures 1 & 5 and col. 4, lines 49-68), that a capacitor (36 or 47) in conjunction with a resistance may be utilized in the triggering of the protective feature composed of transistors. As such, it is the position of the examiner that it would have been obvious to one having ordinary skill in the art to incorporate the teachings of Merrill in that the use of a capacitor for triggering purposes would lend to a less power dissipating design during normal circuit operation while offering responsive triggering during spike conditions.

6. Applicant's arguments have been fully considered but they are not persuasive. With respect to the maintained drawing requirement, Applicant is directed to Figure 3, wherein it is clearly illustrated that the cathode of the diode (D) is connected to the third terminal of the transistor and that the anode of the diode (D) is connected to the second power supply (V-). The bulk of Applicant's remarks concerning the application of Prior Art to the claim language stems around the argument that the amended language of "connected to" versus the old language of "coupled to" no longer allows the Pianka reference to anticipate the claim language under 35 USC 102 (b). However, it is the position of the Examiner that the reference does properly anticipate the claim language. "Connected" includes being joined to another, but is broader than that, in that two things can be "connected" to each other

by way of or through their common connection to something else. -- Kreis AG v. American Hospital Supply corp. (DC NIII) 192 USPQ 585.

The claim language is also open-ended which does not preclude other components. Furthermore, how can Applicant argue with respect to the language of Claim 7 and the application of the Pianka reference that

> "... in order for transistor 201 to have a first terminal coupled to a first supply voltage (VDD) and a second terminal connected to a second supply voltage (VSS), pull-down transistor 202 would have to be eliminated from the circuit."

when Claim 15 has been amended to include that

> "... and a third terminal connected to said first power supply through a capacitor; ...".

Does this mean that the in order for the third terminal to be connected to the first power supply, that the capacitor must be eliminated from the circuit? It is suggested that Applicant incorporate the language, "directly connected" into the claims so as to overcome anticipation by the Pianka reference. As far as the application of Banura and Merrill, the resistors of Banura drop voltages due to current flow and their respective voltage levels with respect to the biasing of transistor (T1) cause it to saturate at a desired time (a triggered time) thereby allowing performance of the protective feature. The capacitors relied upon in the Merrill reference also charge and allow for (a triggered time) so as to offer protection. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the

references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Ronald W. Leja whose telephone number is (703)308-2008.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)308-1782. The Group FAX numbers are (703)305-3431 or (703)305-3432.

RONALD W. LEJA
PATENT EXAMINER
GROUP 2100

9/23/97

RWL
September 23, 1997